REMARKS

Claims 2 and 4 are pending herein. By the Office Action, claims 2 and 4 are rejected under 35 U.S.C. §103(a). Applicants respectfully request reconsideration in view of the following remarks.

I. §103 Rejection

Claims 2 and 4 are rejected under 35 U.S.C. §103(a) over Nakano (US 6004866) in view of Takashi (EP 0928017). Applicants respectfully traverse this rejection.

A. The Invention

The claimed invention is directed to bonded wafers having a base wafer bonded to a bond wafer, and where at least a chamfered part of the base wafer is mirror-polished. The claimed bonded wafers provide significant advantages over single wafers and bonded wafers of the prior art. Thus, important characteristics of the claimed invention are that a chamfered part of the base wafer is mirror surface (claim 2) and a back surface and a chamfered part of the base wafer are mirror surface (claim 4). At least these characteristics distinguish the claimed invention over the cited references.

According to the prior art, bonded wafers were generally produced by either (1) use of grinding and polishing processes or (2) use of hydrogen ions or rare gas ions. See specification at page 1, last paragraph and page 3, line 5 to page 4, line 9. In the first method, one of the wafers, the bond wafer, is subjected to grinding and polishing processes to reduce its thickness to a desired thickness for subsequent fabrication of a device thereon. As a result, a SOI layer is formed on the other wafer, the base wafer. In the second conventional method, hydrogen ions or rare gas ions are implanted into a bond wafer to form a fine bubble layer. The bond wafer is then bonded to a base wafer. A portion of the bond wafer is then delaminated by using the fine bubble layer as a cleavage plane, so that a SOI layer having a very thin and uniform thickness can be provided on the base wafer.

In each of the conventional methods, a bonded wafer is formed by bonding a base wafer and a bond wafer. As such, high flatness of each bonding surface is required. Thus, conventional practice has been to use conventional wafers in which one surface, the bonding surface, is mirror polished. See specification at page 5, lines 1-5 and page 7, lines 9-13.

Producing such bonding surfaces with a high flatness is difficult. One problem that must be addressed is the generation of particles, particularly at a chamfered part of a base wafer. In order to produce a thin film SOI wafer, such as a thin film SOI wafer having a film thickness of 0.1 ± 0.01 μm, it is necessary to apply processing steps such as alkali etching to advanced devices having very fine patterns or special structures. However, when alkali etching is applied to such structures, the problem of generation of particles becomes particularly important, especially at a chamfered part of a base wafer of the SOI wafer. Specification, page 8, line 22 to page 9, line 2. It is believed that such generation of particles arises from uneven shapes resulting from varying etching rates of various exposed orientations of the surface of the wafer. Page 9, lines 2-9.

The present inventors overcame the problems of the prior art by providing a bonded wafer having a base wafer, where a back surface of the base wafer is chemically etched or mirror polished, a chamfered part of the base wafer is mirror surface, and the base wafer is bonded to a bond wafer. In embodiments, the base wafer has a chemically etched back surface on which a maximal depth of pits is 6 μm or less, an average value of waviness is 0.04 μm or less and a power spectrum density is 0.5 to 10 μm^3 as measured by waviness having a wavelength of 10 mm. The present inventors have discovered that such a base wafer provides an SOI layer or silicon active layer that has extremely excellent thickness uniformity. Accordingly, a bonded wafer having the base wafer can be used for fabrication of devices having fine patterns or special structures, and can suppress generation of particles

even from a chamfered part. As a result, manufacturing yield and cost reduction are improved. Specification, page 16, line 23 to page 18, line 15 and page 27, lines 8-11.

B. Claims 2 and 4 Are Patentable Over Nakano and Takashi

Claim 2 is directed to a bonded wafer having a base wafer wherein the base wafer has a chemically etched back surface on which a maximal depth of pits is 6 μm or less, an average value of waviness is 0.04 μm or less and a power spectrum density is 0.5 to 10 μm^3 as measured by waviness having a wavelength of 10 mm, and a chamfered part of the base wafer is mirror surface, wherein the base wafer is bonded to a bond wafer. Claim 4 is directed to a bonded wafer having a base wafer wherein at least a back surface and a chamfered part of the base wafer are mirror surface and the chamfered part of the base wafer is subjected to chamfering and mirror finishing, wherein the base wafer is bonded to a bond wafer. Such bonded wafers are not taught or suggested in Nakano and/or Takashi.

Nakano is directed to a method for manufacturing a bonded wafer comprising the steps of: mirror-polishing a surface of first and second substrates, bringing the mirror-polished surfaces of the substrates into contact with each other to join them, and subjecting the substrates to a heat treatment to firmly bond them. One of the surfaces of the first and second substrates prior to bonding, or one surface of the bonded wafer, is subjected to a polishing treatment for exerting little influence by irregularities on a rear surface of the one substrate or by a figure of a surface of a polishing plate that is in contact with the rear surface of the one substrate. Nakano at Abstract. Nakano thus generally discloses a method for manufacturing a bonded wafer, comprising mirror-polishing surfaces of two substrates, and joining the mirror-polished surfaces of the two substrates together. See Nakano at claim 1; Figs. 1A-1F.

Furthermore, at col. 6, lines 62-64, Nakano describes performing a polishing step on a surface of at least one of the substrates before bonding, or on a surface of the bonded wafer.

Nakano also describes a double-side polishing step, where the front and rear surfaces of the wafer are polished at the same time. See col. 7, lines 11-59. This double-side polishing step can be used to polish the base wafer or a bonded wafer. Col. 8, lines 41-44; Example 1; Table 1.

However, Nakano does not teach or suggest that a chamfered part of the base wafer is mirror-polished, as required by the claimed invention. At most, Nakano only teaches that the bond surface and optionally the back surface of the base wafer is mirror polished.

Takashi does not overcome the deficiencies of Nakano. Takashi is directed to semiconductor wafers. As indicated in the Office Action, Takashi discloses wafers having a maximal pit depth of 6 μm or less and an average value of waviness of 0.04 μm or less. See page 4, lines 44 and 45; paragraph [0034]. These properties are also shown in Takashi in Examples 2 and 3. Page 9, Table 1. Takashi discloses that the wafer can be formed by chamfering, lapping, etching, mirror polishing, and cleaning. See page 3, lines 1-4. The Office Action thus argues that when a bonded wafer is produced by the method of Nakano, but using the semiconductor wafers of Takashi, the result would be the invention of the instant claims. Applicants disagree.

First, Takashi nowhere teaches or suggests that such a wafer in which pit depth and waviness are small is used as a base wafer for a bonded wafer. Thus, there would have been no motivation to combine Nakano and Takashi in the manner asserted in the Office Action.

Second, neither Nakano nor Takashi teach or suggest that the chamfered part of the base wafer is mirror surface. Although Nakano and Takashi individually describe polishing surfaces of the wafer, those disclosures are related only to the main surfaces of a wafer, not to the chamfered surface, as claimed.

Nakano discloses a double side polishing apparatus. See Fig. 3 and col. 8, line 41 to col. 9, line 4. Nakano describes therein that the base wafer is polished in the double side

polishing machine. However, Nakano nowhere teaches or suggests that the machine also polishes the chamfered part of the wafer. In fact, it would be understood by one of ordinary skill in the art that if a base wafer is polished by a double side polishing apparatus as disclosed in Nakano, only both main surfaces of the wafer would be polished; the apparatus could not also polish the chamfered surface of the base wafer. Likewise, Nakano also discloses a single side polishing apparatus. See Fig. 4. However, that apparatus also only polishes one of the main surfaces of the base wafer, not a chamfered part of the wafer.

In an effort to overcome the deficiency of Nakano, the Office Action argues that Takashi discloses a mirror polished chamfered part. The Office Action alleges "Takashi discloses a chamfered part of the base that is mirror polished in order to decrease the depth of the pits to a possible extent (page 5 lines 42-44)." See Office Action at page 5. However, the passage of Takashi relied upon by the Office Action does not support the Office Action's allegation.

Instead, Takashi only discloses at page 5, lines 42-44, that "such pits must be removed through polishing in a subsequent mirror-polishing step, and therefore the polishing stock removal in the mirror-polishing step must be set greater than the maximum value of the depth of such deep pits." That disclosure is related only to polishing the main surfaces of the wafer, not to polishing a chamfered part.

For example, Takashi describes at page 7, lines 26-27, that mirror-polishing must be increased "since deep pits exist and surface roughness (Ra) increases." This disclosure further emphasizes that Takashi's mirror polishing is conducted only on the main surfaces of the wafer, and not on the chamfered part. At most, it would have been obvious for one of ordinary skill in the art to use either the one-sided or two-sided polishing apparatus of Nakano to polish the wafer, and to conduct that polishing at a rate to remove deep pits as

taught by Takashi. However, such processes would still mirror polish only the main surfaces of the wafer, and not the chamfered part.

Neither the wafers of Nakano nor Takashi have a chamfered part of the wafer that is mirror-polished. Even if a bonded wafer is produced using the semiconductor wafer of Takashi as a base wafer in the process of Nakano, the resultant product would not have a mirror-polished chamfered part, as neither reference teaches or suggests to mirror-polish a chamfered part. As a result, the bonded wafer would generate particles, especially at the chamfered part, during subsequent etching processes, causing a lower process yield and higher process costs. The resultant bonded wafer would thus be different from the bonded wafer of the claimed invention, and would not solve the problems addressed by the claimed invention.

For at least these reasons, the claimed invention would not have been obvious over a combination of Nakano and Takashi. Thus, claims 2 and 4 are patentable over Nakano in view of Takashi. Reconsideration and withdrawal of the rejection are respectfully requested.

II. Conclusion

In view of the foregoing remarks, Applicants submit that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the application are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the telephone number listed below.

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Date: June 14, 2005

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